

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 2, line 20 as follows:

In an advantageous embodiment of the invention, the integrated circuit further includes a ~~well~~ frame of a low-resistance or conductive material whose walls surround the inductive element completely, said ~~well~~ frame having at least one slot over its entire height. The inductive element, when positioned in the neighborhood of another inductive element, creates a mutual inductance with this other inductive element. This mutual inductance tends to deteriorate the quality factor of the inductive element. The ~~well~~ frame makes it possible to limit the occurrence of this effect by limiting the magnetic interaction of the inductive element with any other inductive element present in the circuit. A slot is formed over the entire height of the ~~well~~ frame so as to prevent the formation of a current loop at the surface of the ~~well~~ frame. Since the integrated circuit is formed by superposed layers, each made of a low-resistance or conductive material, the walls of the ~~well~~ frame can be formed by a stack of tracks, each formed in one of said layers around a perimeter defined by the surface of the inductive element, said tracks being interconnected. The implementation of the ~~well~~ frame by the use of existing layers

does not lead to an increase in size of the circuit.

Advantageously, the ~~well~~ frame and the conductive layer may be interconnected to the same reference potential terminal, for example the circuit ground, in order to preclude the formation of parasitic capacitances.

Please amend the paragraph beginning on page 3, line 4 as follows:

In a variant of the invention, the integrated circuit comprises two inductive elements, the two being connected between a potential terminal which, depending on the requirements imposed on the circuit, may be either a supply terminal VCC of fixed or variable potential, or a terminal at a reference or ground potential GND, and a terminal which connects the inductive element to a circuit. They are arranged to allow the passage of a current I which flows between said terminals. These two inductive elements are symmetrical and are each formed by a single and similar turn. The choice of the structure of this turn influences the value of the mutual inductance which is formed when a current passes through the turn and, consequently, influences the values of the quality factors of the inductive elements formed with the aid of the turn. This choice is made so as to optimize the quality factors of the inductive elements. Said turn will advantageously be surrounded by a ~~well~~ frame as

described ~~hereinbefore~~ above in order to maximize the reduction of the electromagnetic interactions between said inductive elements and other elements of the circuit.

Please amend the paragraph beginning on page 4, line 11 as follows:

- Fig. 1 is a plan view of an integrated circuit in accordance with an advantageous embodiment of the invention (and shows a frame of an inductive element of the integrated circuit partially broken away),

Please amend the paragraph beginning on page 5, line 8 as follows:

Fig. 2 is a sectional view of an integrated circuit in a preferred embodiment of the invention, taken in a plane defined by A-A in Fig. 1. Said Figure is merely illustrative of a special method of realizing the conductive layer 1 described with reference to Fig. 1. The ~~circuit~~ conductive layer 1 comprises a substrate 7 which may be connected to a reference potential terminal and in which trenches T are formed, which trenches T are perpendicular to the turn of the inductive element 2. The bottoms of these trenches T are covered with a low-resistance or conductive material M. Thus, a conductive layer 1 as shown in

Fig. 1 can be obtained. Finally, these trenches are filled with a ~~high-resistivity~~ high-resistance or insulating material forming an insulating layer R.

Please amend the paragraph beginning on page 5, line 20 as follows:

As a result of its design, the conductive layer P, which is generally made of silicon, has a special structure which meets the requirements imposed on the circuit: since it occupies only a portion of the total area of the circuit, this structure has interstices. In particular, the surface where the inductive element is to be integrated covers such an interstice. A ~~low-resistance~~ high-resistance or insulating material fills these interstices, thereby forming an insulating layer 9 at the same level as the conductive layer P.

Please amend the paragraph beginning on page 6, line 19 as follows:

In the embodiment described here, a ~~well~~ frame 10 made of a conductive material is formed around the inductive element 2. Over its entire height, the ~~well~~ frame 10 has a slot 11, which is indicated by a non-hatched area in ~~the~~ Figure 2, yielding a partial section, which slot interrupts any possible flow of current induced by the inductive element 2 it surrounds. This

~~well~~ frame 10 enables the mutual inductances between the inductive element 2 and circuit elements in the proximity of said inductive element to be minimized. In the embodiment described here, the ~~well~~ frame 10 is realized by junctions of parts of the layers P and M1. ~~Said well~~ The frame 10 is sufficiently high to ensure a proper insulation between the inductive element 2 and the rest of the circuit and thus limit the magnetic interaction. In general terms, each inductive element or part of an inductive element included in the integrated circuit can be insulated by such a ~~well~~ frame, so as to minimize the mutual inductances that may be formed between this inductive element or part of an inductive element and other elements present in the circuit.

Please amend the paragraph beginning on page 6, line 31 as follows:

In a preferred embodiment of the invention, the conductive layer 1 and the ~~well~~ frame 10 are together connected to a reference potential terminal. The parasitic capacitive couplings between the conductive layer 1 and the substrate 7 on the one hand, between the conductive layer 1 and the inductive element 2 on the other and, finally, between the conductive layer 1 and the ~~well~~ frame 10, are thus limited considerably. The inductive elements included in this variant of the integrated circuit in accordance with the invention will then have a high quality

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